A D-BAND MONOLITHIC FUNDAMENTAL OSCILLATOR USING INP-BASED HEMT'S

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Abstract

The design and experimental characteristics of the first fundamental D-band monolithic HEMT oscillator are reported. The circuit is based on a dual feedback topology and uses 0.1 μm pseudomorphic double heterojunction InAlAs/$In_{0.7}Ga_{0.3}As$ HEMT's. It includes on-chip bias circuitry and an integrated E-field probe for direct radiation into the waveguide. An oscillation frequency of 130.7 GHz was measured and the output power level was -7.9 dBm using HEMT's of small gate periphery (90 μm). This represents the highest frequency of fundamental signal generation out of monolithic chips using three-terminal devices.

1 Introduction

Lattice-matched and strained (pseudomorphic) InAlAs/InGaAs HEMT's on InP substrates are recognized as the most suitable components for operation at millimeter-wave frequencies. Discrete devices have demonstrated a high f_{max} of 455 GHz [1] and an f_T of 340 GHz [2]. Pseudomorphic InAlAs/$In_xGa_{1-x}As$ (x>0.53) HEMT's are particularly promising candidates for high-frequency and low-noise applications due to the superior material properties of the strained InGaAs channel. The strained InGaAs channel has larger Γ-to-L valley separation and thus offers higer peak and average velocities compared with lattice matched channels. Pseudomorphic devices may, however, face problems of poor output conductance and limited power performance. These problems can be alleviated by employing a double heterostructure (DH) design. The bottom heterojunction helps to improve carrier confinement and increases the electron density in the channel. As a result, DH-HEMT's show high f_{max} and larger current densities and are therefore very promising for high-frequency oscillator applications.[3]

High frequency monolithic circuits using InP-based HEMT's have started emerging recently and include ultra broadband amplifiers [4] and W-band mixers [5]. InP-based HEMT's have also been used for the realization of monolithic oscillators. Ka-band oscillators were investigated by the authors and showed a record high DC-to-RF efficiency of 36 % at 35 GHz [6] and W-band oscillators operated around 80 GHz with an output power of 1.2 mW using 36 μm gate periphery devices [7]. Various applications such as, for example, space-based remote sensing and radiometry require signal generation above 100 GHz. A fully integrated D-band oscillator-doubler chain has been developed for this purpose, demonstrating an output power of -12 dBm at 132 GHz. [8] Fundamental sources are, however, a preferred solution compared to frequency multiplication techniques. GaAs-based MESFET's and HEMT's have been used as signal sources up to W-band and slightly above [9][10]. These devices may, however, be limited at frequencies well above 100 GHz due to their modest gain.

In this work, we present the design, fabrication and performance of a D-band monolithic fundamental oscillator using pseudomorphic double heterojunction InAlAs/InGaAs HEMT's. The circuit operates at 130.7 GHz with an output power of -7.9 dBm. This represents the highest frequency fundamental signal generation out of a monolithic chip using any type of three-terminal device.

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2 Device Characteristics and MMIC Fabrication

The layer structure of InAlAs/InGaAs HEMT's used in this work is shown in Fig. 1. The HEMT's

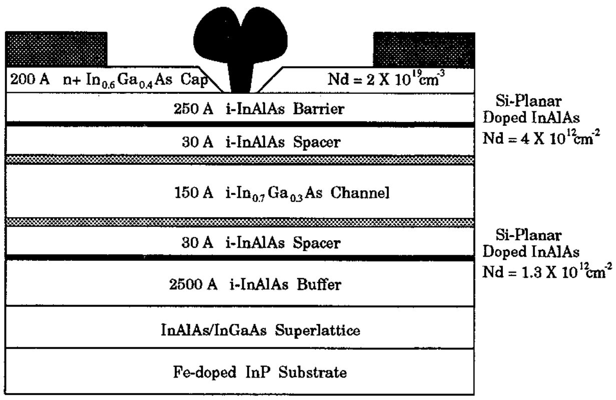

Figure 1: **Layer structure of the pseudomorphic double heterostructure InAlAs/InGaAs HEMT's**

are based on the double heterojunction design (DH) and employ a strained $In_{0.7}Ga_{0.3}As$ channel. The wafer was grown on a semi-insulating InP substrate by MBE at TRW. The structure consists of : i) a 200 Å indium-rich $In_{0.6}Ga_{0.4}As$ cap layer, heavily doped with Si ($2\times10^{19}/cm^3$), for low resistivity ohmic contacts, ii) a 250 Å undoped InAlAs Schottky barrier layer, iii) a top Si-planar doped donor layer with a doping density of $4\times10^{12}/cm^2$, iv) a 30 Å spacer layer, v) an undoped strained $In_{0.7}Ga_{0.3}As$ channel, vi) another 30 Å spacer layer, vii) an additional bottom planar doped layer with a lower doping density ($1.3\ \times10^{12}/cm^2$), and viii) a 2500 Å undoped InAlAs buffer. The 2DEG is formed both at the top InAlAs/InGaAs and the bottom InGaAs/InAlAs heterojunction. The $In_{0.7}Ga_{0.3}As$ channel with 17 % excess indium offers better carrier transport and improved confinement than lattice-matched designs. The bottom heterojunction of DH-HEMT's allows them to have a low output conductance and large current density, which leads to high f_{max} and large power density, respectively. DH-HEMT's are therefore very promising for oscillator applications. The Hall mobility of the layers used in this work was about 9,000 $cm^2/V \cdot sec$ and the carrier concentration was $4.5\times10^{12}/cm^2$ at room temperature.

The D-band monolithic circuits were fabricated using the InP-based MMIC process developed at

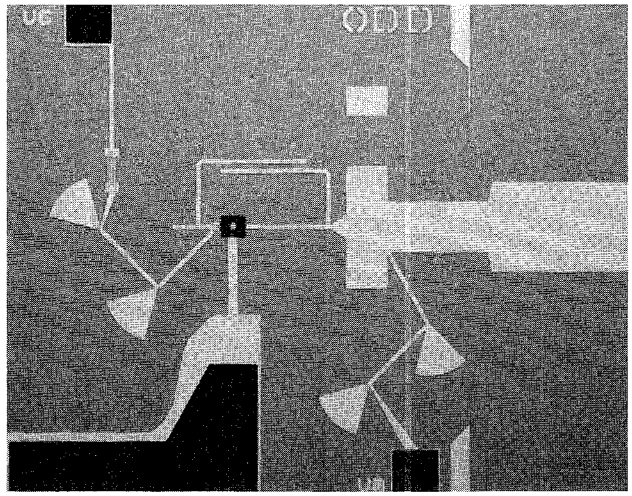

Figure 2: **Photograph of the D-band monolithic HEMT oscillator**

the University of Michigan. Optical lithography was used for all the steps except for the 0.1 μm gate definition where E-beam lithography was employed. The JEOL E-beam lithography system was used to define 0.1 μm long mushroom-shaped gates. The gate recess etching was performed by wet chemical etching and Ti/Pt/Au was deposited as gate metal. The overlay capacitors were realized by lifting off sputtered SiO_2. Interconnects and microstrip elements were realized using evaporated thick Ti/Au (1000/10000 Å). Airbridges were finally formed by electroplated Au. A photograph of the fabricated chip is shown in Fig. 2.

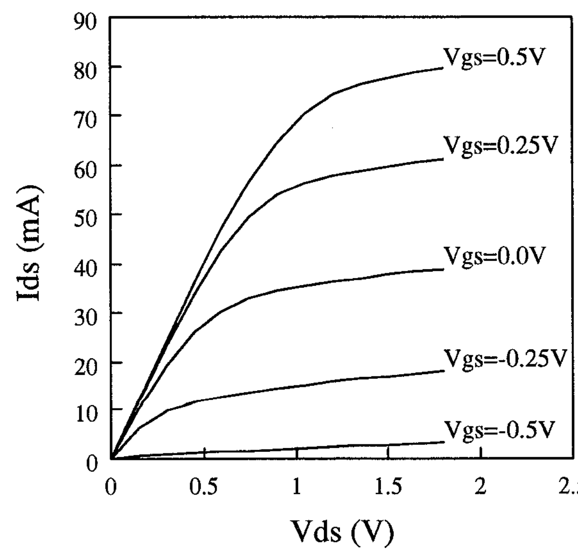

Figure 3: **DC I-V characteristics of the double heterojunction InAlAs/InGaAs HEMT's used in the D-band oscillator (L_g = 0.1 μm, W_g = 90 μm)**

DC characteristics of a typical 0.1 $\mu m \times 90$ μm DH-HEMT are shown in Fig. 3. The devices showed an extrinsic DC transconductance of 1000 mS/mm and a maximum current density close to 1 A/mm. The source-to-drain breakdown voltage was limited to about 2 V for this pseudomorphic design and excellent pinch-off characteristics were found. The I-V characteristics do not reveal the presence of "kink" effect, an effect often observed in pseudomorphic single heterojunction HEMT's due to trapping and detrapping of carriers injected into the InAlAs buffer. The additional bottom heterojunction in the DH design employed in this work, serves apparently as a barrier and prevents the carriers from being injected into the buffer layer, resulting in "kink"-free I-V characteristics and reduced output conductance. The DC output conductance was as low as 46.7 mS/mm and the DC voltage gain (G_m/G_{ds}) was about 21.4. On-wafer probing was performed at the end of the whole MMIC process to evaluate high frequency characteristics of the devices and an extrinsic f_T of 140 GHz and an f_{max} of 270 GHz was found.

3 Monolithic Oscillator Design

The oscillator design was based on both small-signal and large-signal HEMT models. Equivalent circuit elements were extracted from measured multi-bias S-parameters using an analytical approach. Separate "cold" measurements were performed to evaluate the bias independent external elements such as series resistances and pad capacitances. After stripping off the effects of the external elements, the internal elements were calculated analytically. Multi-bias small-signal elements were then used to construct a large-signal model using a 2-D cubic spline technique as described in [5] and [7]. This nonlinear model does not depend on DC parameters which may be quite different from the high frequency values due to frequency dispersion. Accurate device models could in this way be obtained without any fitting and optimization routines.

The oscillator uses a common source HEMT configuration with a dual feedback scheme consisting of a series feedback element from source to ground and a parallel feedback element from drain to gate. The overall gain of this circuit is limited to a small value due to the small gain of the HEMT's in the frequency range of operation (~6dB at 130 GHz for the HEMT's with f_{max}=270GHz used in this work) and the mismatches and losses introduced by the feedback loops and source grounding. The dual feedback topology used for the D-band oscillator permits, however, to maximize the available gain and thus negative resistance, as already demonstrated at Ka-band [6].

The D-band output signal was directly radiated into a WR-5 waveguide using a monolithically integrated on-chip E-field probe. No external microstrip-to-waveguide transition was therefore needed and bonding was avoided on the RF side of the chip. The biasing circuitry consisting of a quarter wavelength line and a radial stub was also integrated on the chip. Stabilization circuits were incorporated both on-chip and off-chip to suppress unwanted oscillations at low frequencies. An on-chip 50 Ω series resistor was added to the gate side and an off-chip capacitor and 50 Ω resistor was used in the drain bias terminal for circuit stabilization.

4 Measured D-band Oscillator Characteristics

The circuit was mounted in an in-house developed test fixture for testing. The fixture has WR-5 waveguide ports and four bias lines. Care was taken to ensure a smooth surface for chip mounting and a movable backshort was used for optimizing the waveguide-fixture transition characteristics. For the detection of the oscillation signal, the output of the test fixture was connected to a power meter through a frequency meter.

The gate bias was first fixed to the value necessary for maximum transconductance. The power and the DC drain current were then evaluated as the drain bias was increased. The chip broke into oscillation at a V_{ds} of 1 V and a drain current decrease by a few mA's was observed when the drain bias was raised from 0.9 V to 1 V. This variation is due to self-biasing caused by the nonlinear gate-source junction conductance as the oscillation builds up. It is interesting to note that this current drop was much smaller than the one observed in lower fundamental frequency monolithic chips such as the Ka-band oscillators reported earlier by the authors [6]. The difference is apparently due to the shorting effect of gate-to-source capacitance, which is more pronounced at high frequencies.

The fundamental signal oscillation of the chip was found to be around 130 GHz. No external tuning was necessary for the circuit operation. The output power and frequency dependence on the drain bias

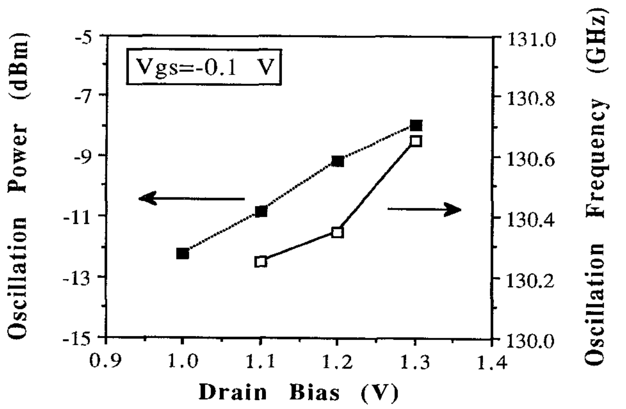

Figure 4: Oscillation power and frequency dependence on the drain bias voltage of the HEMT

voltage are shown in Fig. 4. While the oscillation frequency increases slightly with the drain bias, the oscillation power is found to be a strong function of drain bias voltage and increased from -12.2 dBm to -7.9 dBm as V_{ds} varied from 1.0 V to 1.3 V. The power level obtained from the chip was consistent with the small gate width (2 fingers of 0.1 $\mu m \times$ 45 μm) and low V_{ds} bias operation of the employed devices.

5 Conclusion

The first monolithic fundamental FET oscillator at D-band is demonstrated using submicron pseudomorphic DH-InAlAs/ InGaAs HEMT technology. The circuit design was based on accurate HEMT modeling based on multi-bias S-parameter characterization. The circuit uses dual feedback topology for enhanced negative resistances at D-band. The monolithic chip contained on-chip bias circuitry and an integrated E-field probe for direct signal radiation into a waveguide. The circuit oscillated at 130.7 GHz with an output power of -7.9 dBm at the drain voltage of 1.3 V using 90 μm gate periphery HEMT's. This is the highest fundamental frequency signal generation reported out of monolithic chips using three-terminal devices and demonstrates that InP-based HEMT MIMIC's are promising candidates for monolithic signal sources above 100 GHz.

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